

Optimization of Indium-Lead Alloys for Controlled Collapse Chip Connection Application

Indium-lead solders are used for IBM controlled collapse chip connections (C-4s) to improve fatigue life in temperature cycling for large chip applications. Using 50% In-Pb alloy, which is expensive, has posed a number of manufacturing and reliability concerns. This paper presents the results of development studies leading to the use of a low-indium solder alloy for C-4 applications. This alloy overcomes all previous concerns while exceeding the fatigue life specification of the high-indium alloy. Also described are the variables and tests used to evaluate C-4 performance of In-Pb alloys over the 5% to 50% range. Results are presented graphically and mathematically to show the improvement obtained with indium-content solders over the conventional tin-lead alloys.

Introduction

As semiconductor devices have increased in functional integration and capability, they have grown in size, and the problem of electrically interconnecting them in their first-level packages has become an increasingly significant one. This is especially true for IBM chips which use solder in controlled collapse circuit connections (C-4s) in contrast to individually placed gold or aluminum wires used by most of the industry for individual leads [1-13].

Solder, like all metals, is vulnerable to mechanical fatigue failures caused by different thermal expansion of the chip as compared with that of the ceramic substrate during each on/off cycle over its lifetime. Through the careful development of the technology, C-4 joints have established an industry benchmark for low cost and reliability [14-19]. As chip sizes have grown to almost one centimeter on a side, extending this technology to more severe applications poses a challenge to the metallurgist and packaging engineer.

One of the principal technology innovations in the IBM System/360 computers in the 1960s was the use of solid logic technology (hybrid) modules which provided solder interconnections of several chips in one pass through an oven [7]. These interconnections employed individual copper balls as standoffs [2] to position the chip. However, these copper balls could be deleted because the surface tension of the molten solder of a properly designed joint would afford

adequate mechanical support [8]. Reliability of the joints was ensured by well-designed tests and mathematical modeling [14-19].

By the mid-1970s, the size of chips had exceeded 5 mm, and improved C-4 performance was obtained with the introduction of a 50% In-Pb alloy instead of the tin-lead alloy previously employed [20]. This alloy greatly improved C-4 life, but it resulted in high cost and several reliability concerns, *e.g.*, corrosion [21] and excessive intermetallic formation [22]. These concerns were successfully overcome; however, less costly alternatives for future product applications with even larger chips were clearly needed.

Goldmann *et al.* [20] demonstrated the variation of C-4 fatigue life factors with indium content (Fig. 1). The improvement factors obey a parabolic relationship with an inflection point at 25% indium and rise to $3\times$ (relative to 5% Sn-Pb) at 50% indium. Significantly, at the opposite end of the curve, an $\approx 2\times$ advantage exists for low In-Pb ($\approx 5\%$ indium).

The investigation reported in this paper was launched to develop an alloy that would meet present and future demands for C-4 extension and to take advantage of cost savings inherent with lowered indium composition. The objectives included

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- Lower material costs.
- Reduced wafer manufacturing cycle.
- Module process commonality with 5% Sn-Pb products.
- Lowered quality testing and administration effort.

An intensive study of C-4 performance over a range of indium-lead alloys varying from 5% to 50% indium was initiated. Metal fatigue under temperature cycling was the primary focus, including the influence of cycling frequency. Additionally, the effect of an overcoat for the extension of C-4 fatigue life was studied. Remaining reliability concerns with respect to corrosion [21] were addressed by temperature and humidity tests.

Test results have justified the reduction of indium content for extended-life C-4 applications without loss of fatigue life or compromise of any other reliability objectives for IBM module products.

Data confirm that low-indium C-4s also eliminate the possibility and effects of pad corrosion and excessive inter-metallic (Cu_3In_4) conversion of the pad-limiting metallurgy noted by Goldmann and co-workers [20].

This paper is divided into three principal sections: experimental variables including process parameters, experimental results, and a discussion including equations for C-4 fatigue life variations with indium content.

Experimental variables

For a single chip and substrate configuration, the temperature excursion (ΔT) and the cycling frequency are the only variables. For consistency with existing data bases, the temperature cycling range was 0–100°C. Cycling frequency was varied as explained below.

A large chip was selected to reduce temperature cycling time. The chip footprint provided 130 C-4 pads, of which approximately 40 had to be used for measurement. Testing and statistical methodology, including failure criteria, generally followed methods described by Goldmann *et al.* except for the use of three-point resistance measurements.

All modules used in this investigation were metallized ceramic (MC), with Cr-Cu-Cr interconnection lines, on 28-mm (1.1-in.) 96% aluminum-oxide substrates [4]. All modules were quasihermetic, using an epoxy backseal [5]. The C-4 alloy and substrate overcoat were variables.

Statistical treatment

Solder joint fatigue is generally considered to be a wear-out mechanism which follows a useful life for which the instantaneous failure rate is vanishingly small. Joint failure for this wear-out phase is generally considered to be log-normally

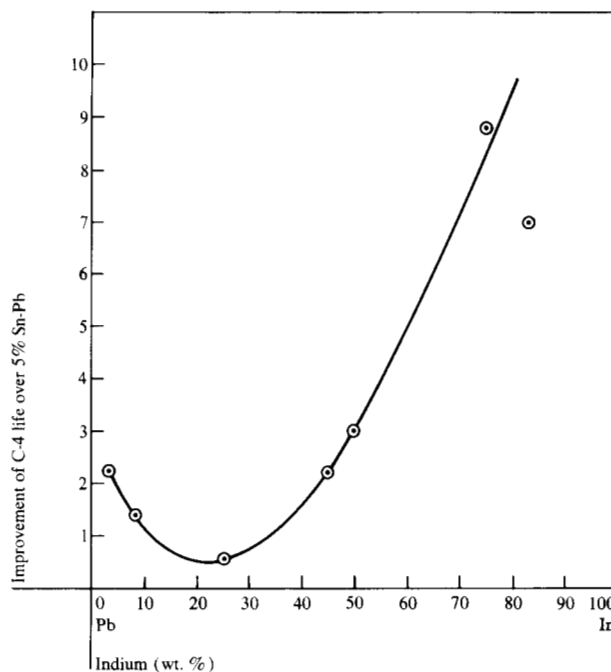


Figure 1 Effect of indium on improvement of C-4 life in temperature cycling (0–100°C, 72 cpd) (data from Ref. 20 replotted—after Goldmann *et al.*).

distributed. Thus the number of temperature cycles to the median of cumulative failures (N_{50}) is a useful parameter for the comparison of technological variables (i.e., alloy content overcoat, etc.). However, N_{50} values are of little use in application forecasts since the tolerable level of device failures is less than 0.1% (i.e., a failed C-4 is equated to a failed device). Thus the value $N_{0.1}$ (the number of cycles to 0.1% cumulative failures) is a more meaningful number. It reflects the combined influence of N_{50} and the standard deviation, sigma (σ), a measure of the dispersion of data. Sigma is often profoundly affected by a technology which causes greater dispersion of the data. The magnitude of sigma also determines the spread of confidence limits, which are 90% for the purpose of this paper.

Alloy variations

Solder alloys of 5%, 10%, 15%, 25%, 35%, and 50% indium (the remaining percentages were lead) were used in this study. Actual C-4 compositions are several percentages lower due primarily to a geometric effect [20]. Analysis of the as-deposited pads was performed by atomic absorption. C-4 temperature cycling data are plotted versus actual In content. To provide a control against which to measure C-4 performance enhancement, 5% Sn-Pb was included as a variable.

Methods for evaporation and processing wafers generally followed procedures described by Goldmann [20].

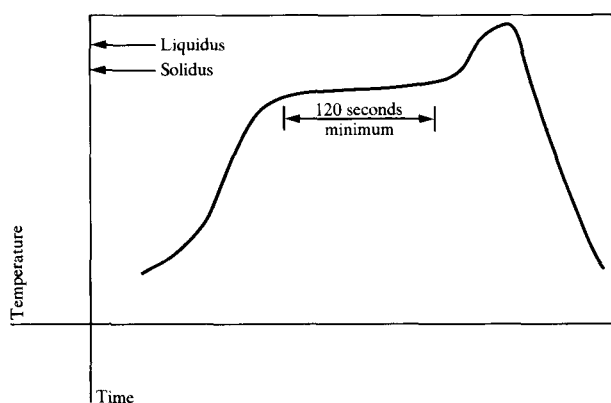


Figure 2 Chip-joining profile schematic.

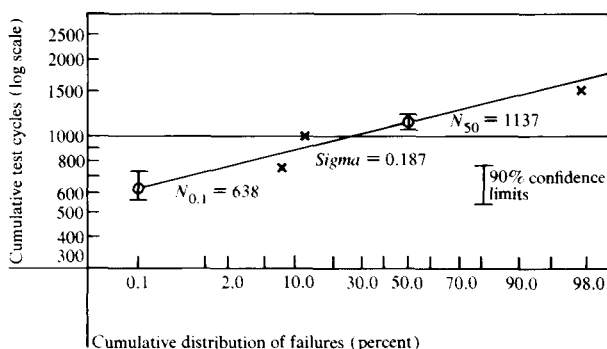


Figure 3 Log-normal plot of C-4 performance of 5% In-Pb without overcoat.

• Overcoat

Substantial improvement of C-4 performance can be gained from proper choice of the overcoat. IBM products currently use polyamide-imide copolymer, which may enhance the life of C-4s without overcoat by more than 2 $\times$. This improvement is believed to result from mechanical reinforcement that may increase C-4 fatigue life as a function of temperature cycling frequency.

• Influence of frequency

Because solders spend much of their working lives in a creep rupture temperature regime, Norris and Landzberg [15] found that frequency is a major factor in C-4 life. They determined an exponential relationship

$$N_{50} \propto f^n,$$

where f = temperature cycling frequency, and $n = 0.33$ for 5% Sn-Pb C-4s.

Similarly, it was determined that 50% In-Pb C-4s have a frequency exponent $n = 0.23$ [23]. Since both exponents were derived with bare C-4 alloys (without overcoat), it was decided that this investigation should focus on actual product configurations that seldom omit the overcoat.

Accordingly, fully overcoated modules were used for the frequency variables study. Testing frequencies ($\Delta T = 0-100^\circ\text{C}$) were 9, 18, 36, and 72 cycles per day (cpd). Prior experience had established that the frequency models were valid between 6-72 cpd for 5% Sn-Pb and 18-72 cpd for 50% In-Pb with uncoated C-4s [15, 23].

• C-4 corrosion

Because the chemical activity of solid-solution alloys varies with concentration of the susceptible element, it was anticipated that low In-Pb alloys would approximate the corrosion behavior of pure lead or 5% Sn-Pb. To demonstrate the dependence of C-4 corrosion on indium content, fully encapsulated modules having all alloy variations, including 5% Sn-Pb, were screened by temperature and humidity testing.

Modules were stressed at 70°C and 70% relative humidity for 6000 hours. X-ray radiography was employed to determine corrosion penetration. Cross-section metallography was employed to confirm radiographic indications.

• Processing

Fabrication of the MC module [20] varied only in chip-joining temperature. Liquidus temperatures increased with higher C-4 lead content. Peak temperatures were selected to exceed liquidus temperatures by approximately 20°C . The chip-joining profiles afforded a preheat plateau in the vicinity of the solidus temperature, followed by a peak, as shown in Fig. 2.

Substrates had the usual 10% Sn-Pb-tinned fingers. Goldmann had shown that the contribution of tin from the land influences C-4 composition and, therefore, lifetime by a negligible margin. This was assumed to be a constant factor in C-4 life results.

Experimental results

Experimental results for the uncoated cells are summarized in Table 1, giving the variation of N_{50} and sigma with indium composition. Figure 3 presents a typical log-normal plot of the cumulative number of test cycles to failure versus cumulative percent failed modules for 5% In-Pb.

Results for the effects of indium concentration on C-4 life variation are given in Fig. 4, which also includes a curve for overcoat as a variable. These curves are generally parabolic with minima in the vicinity of 15% In.

Table 1 Effect of indium composition on C-4 performance, with-out overcoat (0–100°C at 72 cpd).

C-4 composition		N_{50}	Sigma	$N_{0.1}$
Nominal	Actual*			
50% In-Pb	43.8	2,504	0.629	358
35% In-Pb	34.4	1,137	0.162	690
25% In-Pb	21.7	864	0.160	527
15% In-Pb	11.6	762	0.222	384
10% In-Pb	5.0	844	0.252	387
5% In-Pb	3.6	1,137	0.187	638
5% Sn-Pb		701	0.395	206

*Atomic absorption analysis.

• Influence of temperature cycling frequency

To obtain the frequency exponent (n), the C-4 life parameter (N_{50}) is plotted against frequency on log-log paper. If the points are aligned, the slope of the resulting line through them is the frequency exponent. Figure 5 represents such a plot of N_{50} versus frequency for the 25% In alloy (solid curve). This plot is typical of those for all alloys studied, including 5% Sn-Pb. Here, N_{50} decreases from 3000 cycles at 72 cpd to 1500 cycles at 36 cpd. Because the 18-cpd value of N_{50} exceeded that for 36 cpd, some concern was voiced that a least-squares regression might perhaps produce a reasonable exponent n .

Data for all alloys, including 5% Sn-Pb, were investigated by linear regression to determine the validity of the shape of the curve presented in Fig. 5. Not only were the correlation coefficients low, but a statistical test of significance for the slopes supported the shape of the curve shown here. It was therefore concluded that Fig. 5 is representative of all alloys studied. Because these data do not fit the dashed lines representing existing models, it was concluded that 36-cpd and lower frequencies are representative of machine conditions. Accordingly, N_{50} and $N_{0.1}$ values at operating frequencies represent 50% derating of these parameters obtained in 72-cpd tests. These findings confirm those of Sullivan [24, 25], who found that 36 cpd is the equivalent of machine frequency for 5% Sn-Pb C-4s.

Figure 6 presents a comparison of N_{50} s obtained at 72 cpd with those for 36 cpd for all alloy compositions. The 36-cpd curve generally follows the same shape factor. Thus, one may postulate that temperature cycling at 36 cpd is essentially equivalent to that for machine frequencies for the alloys studied.

• Corrosion evaluation

Radiographs of modules subjected to temperature and humidity exposures were screened for corrosion penetration. As expected, 50% In-Pb cells showed extensive corrosion for times exceeding 3000 hours. Also, uncoated cells exhibited

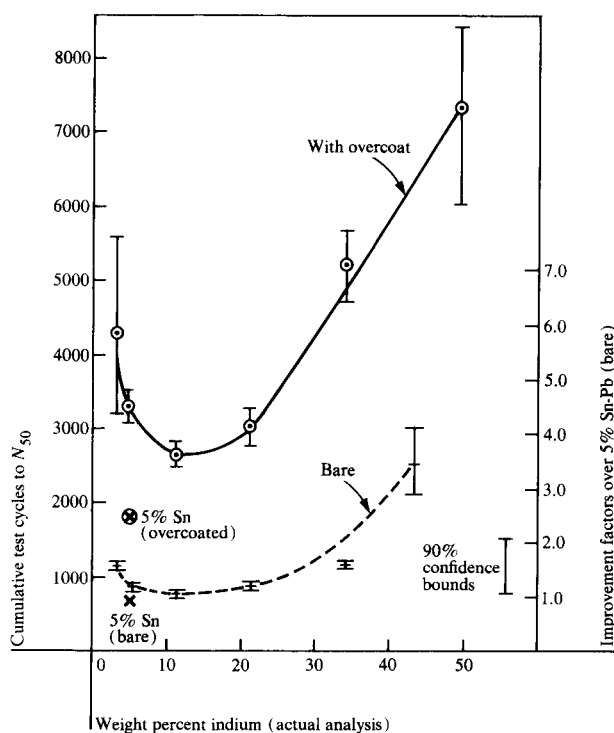


Figure 4 Variation of N_{50} with indium concentration (wt. percent) (0–100°C at 72 cpd).

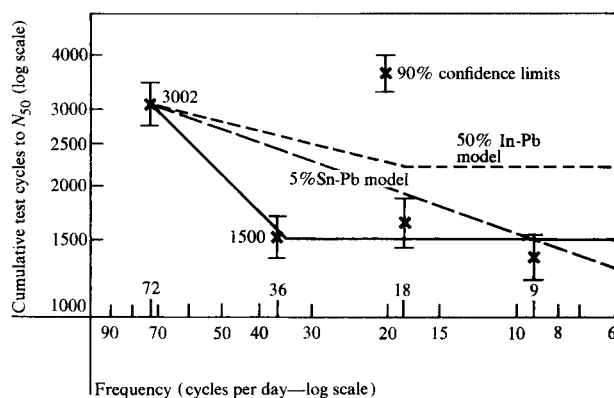


Figure 5 Effect of frequency: N_{50} versus frequency—25% In-Pb C-4s with polyamide-imide topseal.

more corrosion penetration than overcoated parts. Frequency and severity of corrosion indications decreased rapidly with indium concentration and were considered negligible below 25% indium. Cross-section metallography confirmed this finding on 3.6% In-Pb modules exposed for 6000 hours. Examples of typical C-4s for 3.6% and 43% indium are shown in Figs. 7 and 8.

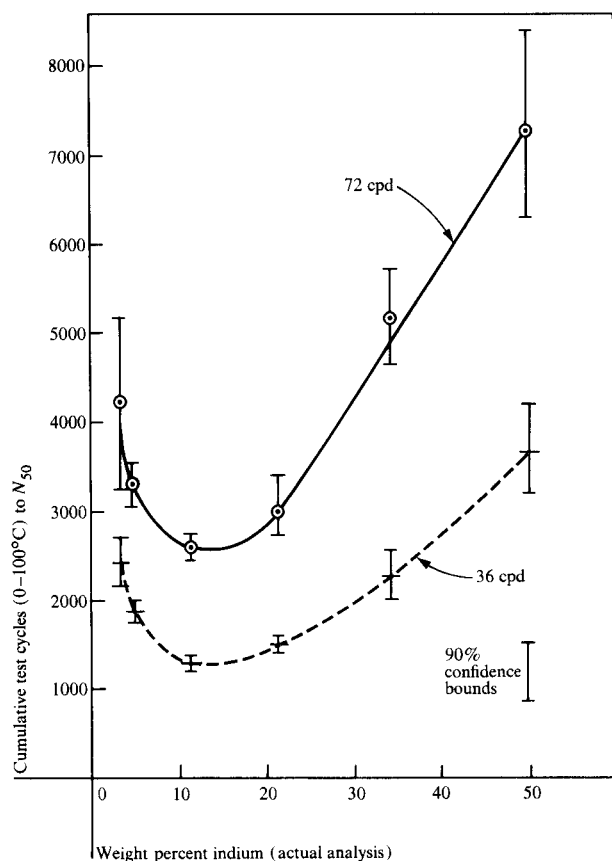


Figure 6 Variation of N_{50} with indium concentration (overcoated chips) at 72 and 36 cpd.

• Process evaluation

Effects of the chip-joining process are compared in Figs. 9 and 10. Figure 9 demonstrates pad-limiting metallurgy (PLM) breakup in 43% In-Pb, also shown in Reference 20, Fig. 5. An exceptionally "clean" PLM configuration with residual copper is exhibited by 3.6% In-Pb, despite a higher chip-joining temperature (355°C versus 260°C) shown in Fig. 10.

Discussion

The primary objective of this investigation was to extend the work of Goldmann [20] relative to the improvement of C-4 performance at low-indium concentrations, as shown in Fig. 1. Figures 4 and 6 show that these curves have a parabolic shape, thus confirming Goldmann's findings. The performance at low-indium levels confirms Goldmann's expectations, but also extends them to actual product configurations with overcoated C-4s. More recent studies with small chips have also substantiated this improvement factor.

It would be useful to provide improvement factors by which fatigue life performance of all indium-lead C-4s may

be estimated by comparing to a measured benchmark (e.g., unencapsulated 5% Sn-Pb C-4s) for which considerable data are available for many chip sizes. Figure 4 (right-side scale) shows improvement factors (IFs) versus indium alloy content (i.e., multipliers for C-4 performance over 5% Sn-Pb). IFs may be estimated with or without overcoat, given the corresponding 5% Sn-Pb parameters for a given chip size. Curves were fitted to the data points for each configuration.

Equations representing these curves are

1. Bare C-4

$$IF = 1.03 + 4.426 \times 10^{-3} (x - 15)^2,$$

2. Polyamide-imide overcoat:

$$IF = 3.55 + 1.058 \times 10^{-2} (x - 15.5)^2,$$

where x = weight percent indium.

Inspection of Fig. 4 reveals an improvement factor of 3.6 for overcoated C-4s with 15% In. At a low-indium percentage, the value is $\approx 5.7\times$.

Conclusions

Conclusions from this study are the following:

1. All cells demonstrated log-normal distribution of fatigue fails as expected.
2. Medians (N_{50} s) of these distributions varied parabolically with indium composition. The minimum for overcoated and bare C-4s occurred at 15% for bare C-4s and 15.5% for overcoated C-4s.
3. Improvement factors relative to bare 5% Sn-Pb C-4s were calculated for bare and overcoated C-4s.
4. Achievable improvements over bare 5% Sn-Pb C-4s by substitution of low indium (3–5% In) is at least 1.6 times ($1.6\times$) without topseal.
5. Enhancement of C-4 fatigue life (at N_{50}) for low In-Pb is $\approx 5.0\times$ over bare 5% Sn-Pb C-4s. This value is contrasted with the generally accepted $2\times$ for polyamide-imide with 5% Sn-Pb.
6. Standard deviations (sigmas) for low-indium composition (bare C-4s) are low, falling within the range of $\sigma = 0.2 \pm 0.05\%$.
7. The effect of frequency variations departed significantly from existing models. For all alloys, N_{50} s at 36 cpd were approximately 50% of those at 72 cpd (the customary testing frequency). Below 36 cpd, N_{50} s were substantially invariant.
8. Corrosion of C-4 pads was virtually nonexistent for compositions below 20% In.
9. Pad-limiting metallurgy intermetallic conversion was greatly reduced with low-indium C-4s.

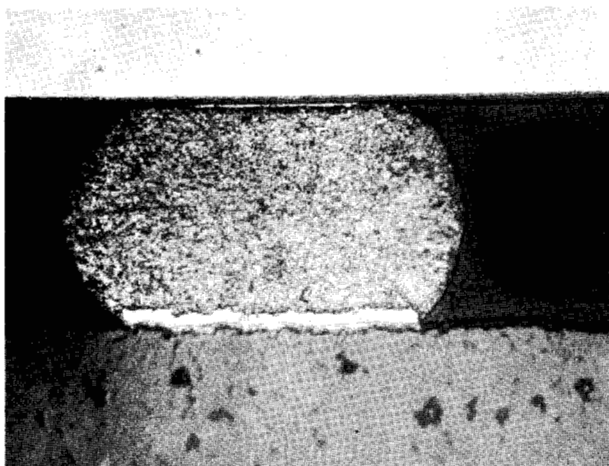


Figure 7 Cross section of 3.6% In-Pb C-4 after exposure to 70°C–70% relative humidity for 6000 hours. Note absence of alloy corrosion. Original magnification: 400 $\times$.

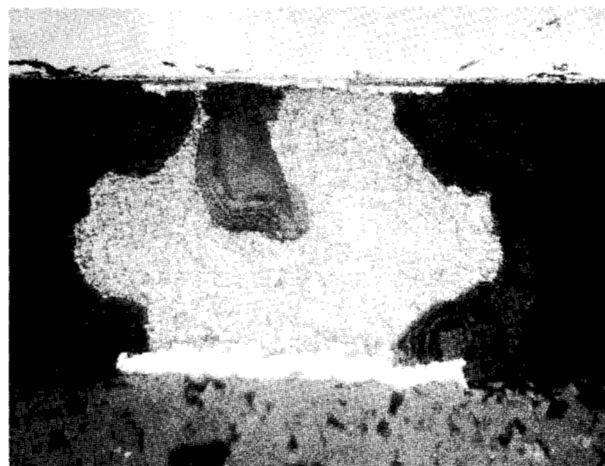


Figure 8 Cross section of 43% In-Pb C-4 after exposure to 70°C–70% relative humidity for 6000 hours. Corrosion penetration is typical for this alloy. Original magnification: 400 $\times$.

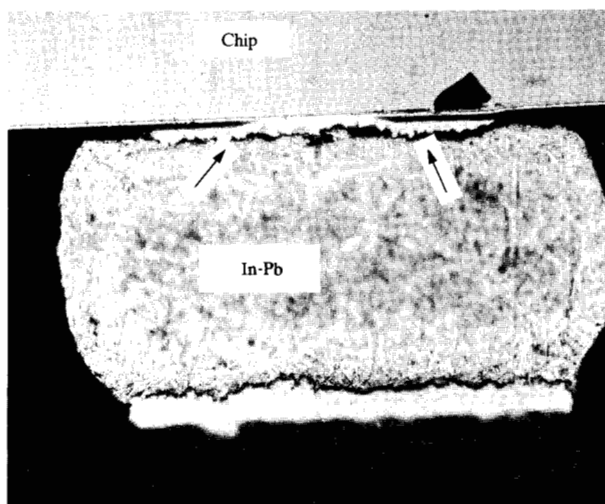


Figure 9 Cross section of 43% In-Pb C-4 after chip joining at 260°C maximum. Fracture mode is typical for high In-Pb alloy. Note excessive intermetallic conversion at pad-limiting metallurgy. Original magnification: $\approx$ 450 $\times$.

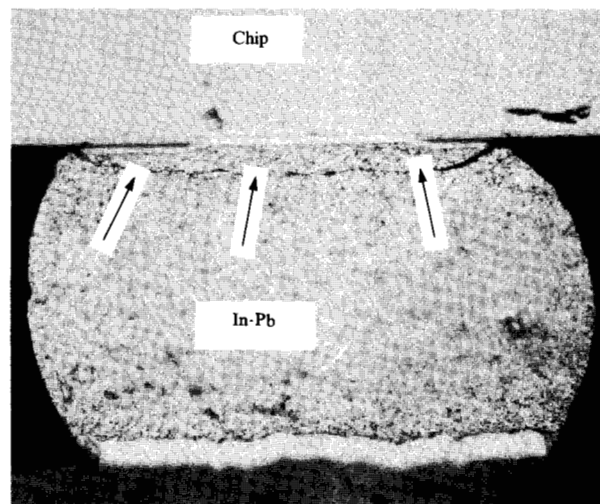


Figure 10 Cross section of 3.6% In-Pb C-4 after chip joining at 354°C. Note low level of intermetallics at pad-limiting metallurgy. Fracture mode is typical for low In-Pb alloy. Original magnification: $\approx$ 450 $\times$.

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